Remarks/Arguments

This amendment is submitted in response to the Office Action mailed July 10, 2003. Reconsideration is respectfully requested.

Claims 1-27 were examined, and all were rejected. Specifically, Claims 1-6 and 8-12 were rejected under 35 U.S.C. Section 102(b) as anticipated by US 4,484,244 – Avery. Claims 11-17 and 19 were rejected under 35 U.S.C. Section 102(b) as anticipated by US 4,876,620 – Borkowicz. Claims 7, 18, and 23 were rejected under 35 U.S.C. Section 103(a) as unpatentable over Avery in view of Borkowicz. Claims 11-27 were rejected under 35 U.S.C. Section 112, second paragraph, as being indefinite, but Claims 20, 21, 22, 24, and 25 were held to define allowable subject matter. In addition, Claims 14 and 20 were objected to for informalities.

In response to the Office Action, Claims 1 and 11 have been amended, Claims 7, 8, 13, and 16-18 have been cancelled, and new claims 28-31 have been added. As explained below, it is respectfully submitted that Claims 1-6, 9-12, 14, 15, and 19-27, as amended, are allowable over the art of record, as are new Claims 28-31.

Claims 11, 12, 14, 15, and 19-27 were rejected under 35 U.S.C. Section 112, second paragraph, as being indefinite. The Examiner contends that it is unclear what the Applicant considers as the "gate" of the SCR that is represented by the combination of the two bipolar transistors TR1 and TR2. Tis rejection is respectfully traversed. Applicant respectfully submits that those skilled in the pertinent arts would recognize that that the base of either of the transistors could be used as the SCR gate, depending on whether one wanted a P-gated SCR or an N-gated SCR, both of which are described in the specification.

Specifically, in the embodiments of Figures 2a and 4a, the gate of the SCR is either the base of TR1 or the base of TR2. In the embodiment of Figure 6, the gate of both the left side SCR and the right side SCR are the bases of the corresponding NPN transistors TR1, TR3. In the embodiments of Figures 7 and 9a, the SCR on the right is gated via the base of the NPN transistor TR1, and the SCR on the left is gated via the base of the PNP transistor TR4. Where gating is achieved via the base of an NPN transistor, the SCR is said to be P-gated, and where gating is achieved via the base of PNP transistor, the SCR is said to be N-gated. It would thus be clear to those skilled in

the pertinent arts what the applicant would consider to be the gate of each SCR described in the specification and drawings.

Accordingly, it is respectfully submitted that Claims 11, 12, 14, 15, and 19-27 fulfill the requirements of 35 U.S.C. Section 112.

From the foregoing discussion, it will be seen that the drawings already show the SCR gate recited in Claims 11 and 20. For example, Figure 2a shows that the SCR formed by the bipolar transistors TR1 and TR2 has a gate that is either the base of TR1 or the base of TR2, depending on whether the SCR is to be P-gated or N-gated, as discussed above. Accordingly, it respectfully submitted that no drawing corrections are needed.

Claims 1-6 and 9-12 were rejected as anticipated by Avery. Claims 11, 12, 14, 15, and 19 were rejected under 35 U.S.C. Section 102(b) as anticipated by Borkowicz. Claim 23 was rejected under 35 U.S.C. Section 103 as unpatentable over Avery in view of Borkowicz. As discussed below, it is respectfully submitted that these claims, as amended, now define patentably over these references.

With respect to Claims 1-4, the Examiner refers to Fig. 2 of Avery, which discloses a circuit for protecting against negative and positive transients. The circuit comprises an SCR (Q3, Q4 and Q1, Q2) for each transient, connected in anti-parallel, and a current-sensing resistor 20 for triggering turn-on. Both the negative and positive transient protectors are, however, current-triggered and not voltage triggered. The Figure 1 circuit in Avery, which is described in Column 2, line 26 to Column 3, line 41 of the reference, operates by voltage-triggering only.

Thus, Avery describes either voltage-triggering at two different voltage magnitudes, or current-triggering at two different voltage magnitudes, but it does not suggest voltage-triggering at a first voltage magnitude and current-triggering at a second voltage magnitude.

Claim 1 has been amended by incorporating into it the limitations of Claims 7 and 8 (which have been cancelled). Claim 1, as amended, thus now defines first trigger means that is voltage-triggered by voltages exceeding a first magnitude on the conductor, and that is current-triggered by a current trigger element in response to voltages exceeding a second magnitude on the conductor, wherein the current trigger

element comprises first and second parallel resistive elements and is connectable in series with the conductor. Thus, Claim 1, as amended, recites a trigger means that is both voltage-triggered and current-triggered, while Avery, as discussed above, discloses either current-triggering only or voltage-triggering only.

Claim 1, as amended, further defines the current trigger element as comprising first and second parallel resistive elements. The Examiner concedes that Avery does not suggest this limitation, and cites Borkowicz as being combinable with Avery to render the claimed combination obvious. While Borkowicz teaches the use of parallel resistive elements 46a and 46b in Fig. 4, it is believed that this parallel resistor arrangement is purely an artifact of having the two thyristors 42 and 44 (which may be analogized to SCRs) arranged back-to-back, and does not contribute in any way to the switching of one thyristor (SCR) or the other. Thus, the parallel resistors of Borkowicz do not constitute a current triggering element, as defined in Claim 1, and there is no suggestion (absent hindsight) to combine the teachings of Borkowicz with the teachings of Avery to provide parallel resistors as a current-triggering element in the circuit defined in Claim 1.

It is therefore respectfully submitted that Claim 1, as amended, defines patentably over Avery, either by itself or in combination with Borkowicz. Claims 2-6, 9 and 10, which depend from Claim 1, likewise define patentably over these references.

Claim 11 has been amended by incorporating therein the limitations of Claims 13, 17, and 18, which have been cancelled. Thus, Claim 11 now defines a first trigger comprising a current trigger element for current triggering the first SCR when the voltage on the conductor exceeds the second magnitude, wherein the current trigger element comprises first and second parallel resistive elements and is connectable in series with the second conductor. Accordingly, it is respectfully submitted that Claim 11 is patentable over either Avery or Borkowicz by themselves, or Avery taken with Borkowicz, for the reasons stated above with regard to Claim 1. Claims 12, 14, 15, 19-21, and 23-27 depend from Claim 11, and should likewise define patentably over these references.

The objections to Claim 14 and 20 have been overcome by, respectively, amending Claim 11 to incorporate the subject matter of Claim 13, and amending Claim

20 to correct the spelling of "gate."

Claims 20-22, 24, and 25 were held to define allowable subject matter. Accordingly, new independent Claim 28 is submitted to present the patentable subject matter of Claim 21 in independent form. (Claim 22 has been amended to depend from new Claim 28.) Similarly, new independent Claim 29 presents the patentable subject matter of Claim 24 in independent form, and new independent Claim 30 presents the patentable subject matter of Claim 25 in independent form. Accordingly, it is respectfully submitted that new claims 28-30 define patentably over the art of record.

New independent Claim 31 defines the subject matter of amended Claim 11, with the added limitation of a diode connected in antiparallel between the cathode and anode terminals of the SCR, wherein the diode provides overvoltage protection at a third discrete voltage magnitude that is of opposite polarity to the first and second discrete voltage magnitudes. It is respectfully submitted that Claim 31 defines patentably over the cited references.

Avery admittedly discloses a diode 22 in Fig. 2. The diode 22 in Avery is, in fact, the emitter-base diode of the transistor Q3 (see Column 3, line 65 to Column 4, line 3), and is therefore an inherent part of the semiconductor structure (see Column 3, lines 61-63). The diode 22 serves to trigger the negative transient protection circuit, which then switches to carry any surge current.

In the subject invention, as defined in Claim 31, the antiparallel diode is a separate diode that protects against transient voltages in the opposite polarity to those protected against by the main SCR. In Figures 2a and 4a, for example, the diode D2 provides protection against positive transients relative to the reference potential, while the SCR provided protection against negative transients. The diode 22 of Avery, by contrast, does not, by itself, protect against transients; rather, it is merely used to trigger the negative transient protection circuit (see Column 3, line 65 to Column 4, line 17).

Thus, neither Avery by itself, nor Avery in combination with Borkowicz, teaches or suggests an antiparallel-connected diode serving the overvoltage protection function defined in Claim 31. Claim 31, therefore, is respectfully submitted to be patentable over the art of record.

Finally, a revised Abstract is submitted herewith, which overcomes the objection stated by the Examiner.

In summary, it is respectfully submitted that Claims 1-6, 9-12, 14, 15, and 19-31, as amended, define patentably over the art of record and should be allowed. Passage of the application to issue is therefore earnestly solicited.

Respectfully submitted,

KLEIN, O'NEILL & SINGH, LLP

Howard J. Klein, Reg. No. 28,727
2 Park Plaza, Suite 510
Irvine, CA 92614
Tel: 949 955-1920
Fax; 949-955-1921